IN THE DRAWINGS

The attached sheets of drawings include changes to Figs. 62 and 72. These sheets, which include Figs. 62 and 72, replaces the original sheets including Figs. 62 and 72.

Attachment: Replacement Sheets (8)

REMARKS

Favorable reconsideration of this application, in view of the present amendments and in light of the following discussion, is respectfully requested.

After entry of this amendment, Claims 1-24 are pending. However, Claims 1-9, 13 and 14 have been withdrawn from further consideration in a previous response. Claims 10 and 12 are amended, and Claims 15-24 are newly added. No new matter is introduced.[1]

In the outstanding Office Action, Figures 62 and 72 were objected to; Claims 10 and 12 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamazaki (U.S. Patent No. 6,765,594) in view of Tam (U.S. Patent Application Publication No. 2002/0021293); and Claim 11 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamazaki and Tam in further view of Miyazima (U.S. Patent Application Publication No. 2002/0171086).

Initially, replacement sheets for Figures 62 and 72 are submitted herewith to address the informalities identified in the outstanding Office Action. Accordingly, it is respectfully requested that the objection to Figures 62 and 72 be withdrawn.

With respect to the rejection of Claims 10 and 12 as being unpatentable over Yamazaki in view of Tam, Claim 10 is amended to recite, *inter alia*, an EL display apparatus that includes:

> a first wiring formed on the substrate and *located under the source driver IC*;
> a second wiring electrically connected to the first wiring and *formed between the source driver IC and a display area*; and
> an anode wiring that branches from the second wiring and configured to apply an anode voltage to the pixels in the display area, a current being supplied to the EL elements via the anode wiring. (Emphasis added.)

Turning to the primary reference, Yamazaki describes an active matrix display that includes a volatile memory (SRAM) to prevent a reduction of an electric charge stored in a

[1] Non-limiting support for the amended claims and the new claims may be found at least at paragraphs [1448]-[1497] of the specification.

gate electrode of an EL driver TFT.[2] More specifically, Yamazaki illustrates a pixel circuit of an EL display as including a data signal line (107) connected to a source of the switching TFT (105), a gate signal line (106) connected to the gate of the switching TFT (105), and SRAM (108) connected between the switching TFT (105) and an EL drive TFT (109) to which an EL element (111) is connected.[3] A gate signal input to the gate signal line (G1) (106) turns on the switching TFT (105), while a data signal input to the source data line (107) supplies image information to the EL drive TFT (109) to correspondingly drive the EL element (111).[4] The SRAM (108) stores the data signal input to the source signal line (107) to prevent loss of the image data due to leakage currents in the EL drive TFT (109).[5]

The outstanding Office Action identifies the gate signal line (106) and source data line (107) as respectively corresponding to the claimed first and second wirings. However, Yamazaki does not describe that the source data line (107) is located under source signal side driver circuit (102) or that the gate signal line (106) is formed between the source signal side driver circuit (102) and a display area. Instead, Yamazaki merely describes the functionality of the gate signal line (106) and the source data line (107), without describing their physical locations relative to each other, a display area, and/or the source signal side driver circuit (102). Conversely, amended Claim 1 recites that the first wiring is formed on the substrate and located under the source driver IC, and also recites that the second wiring is electrically connected to the first wiring and formed between the source driver IC and a display area.

Further, amended Claim 10 requires that the second wiring be electrically connected to the first wiring. However, Yamazaki illustrates that the gate signal line (106) is connected to the gate of switching TFT (105) while source data line (107) is connected to the *source* of

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[2] Yamazaki at column 4, lines 8-26.
[3] Yamazaki at column 8, line 65 – column 9, line 9; see also Figure 3.
[4] Yamazaki at column 10, lines 56-66.
[5] Yamazaki at column 10, line 66 – column 11, line 31.

switching TFT (105).[6] Yamazaki also describes that gate signal line (106) is used to turn switching TFT (105) on while source data line (107) is used to supply a data signal to the EL driver TFT (109) and ultimately the EL element (111).[7] In other words, Yamazaki describes the gate signal line (106) as a mere control line for the switching TFT (106) and the source data line (107) as the supplier of data to the EL driver TFT (109) via the switching TFT (105). Nothing, however, in Yamazaki describes that the data signal of the source data line (107) is supplied to the gate signal line (106), much less that the gate signal line (106) and the source data line (107) are electrically connected. Conversely, amended Claim 10 recites a second wiring electrically connected to the first wiring.

As first recognized by the present inventors, the claimed first and second wirings synergistically combine with the other recited features in amended Claim 10 to reduce brightness irregularities of the EL display by increasing the size of the first wiring to reduce its corresponding resistance, while preserving a small bezel size.[8] Therefore, Yamazaki fails to disclose the claimed first and second wirings, and Tam does not cure this deficiency in Yamazaki. Consequently, no combination of Yamazaki and Tam describes every feature recited in amended Claim 10 and amended Claim 10 is believed to be in condition for allowance, together with any claim depending therefrom. Accordingly, it is respectfully requested that the rejection of Claims 10 and 12 under 35 U.S.C. § 103(a) be withdrawn.

As the rejection of Claim 11 relies upon Yamazaki for describing the above-distinguished features, and the above-distinguished features are not disclosed or suggested by Yamazaki, alone or in combination with any other art of record, it is respectfully submitted that a *prima facie* case of obviousness has not been presented. Accordingly, it is respectfully requested that the rejection of Claim 11 under 35 U.S.C. § 103(a) be withdrawn.

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[6] See Figure 3 of Yamazaki and the associated discussion at column 8, line 65 – column 9, line 9.
[7] Yamazaki at column 10, lines 56-66.
[8] See, e.g., the specification at pages 388-392.

In addition, new Claims 15-24 recite features not disclosed in any art of record, and are thus believed to be in condition for allowance.

For the reasons discussed above, no further issues are believed to be outstanding in the present application, and the present application is believed to be in condition for formal allowance. Therefore, a Notice of Allowance for Claims 10-12 and 15-24 is earnestly solicited.

Respectfully submitted,

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